The Study of MOSFET Parallelism in High Frequency DC/DC Converter

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***Abstract*—The study of MOSFET parallelism and the impact on body diode conduction loss of the switch are presented in this paper. The simulation is carried out for synchronous rectifier buck converter (SRBC) in continuous conduction mode where several configurations of the MOSFET connected in parallel are applied. It is found that the body diode conduction loss has been reduced of more than 35 % in four-parallel S_1 with one S_2 compared to the single pair totem-poled switched SRBC circuit.**

***Index Terms*— Body Diode Conduction Loss, Continuous Conduction Mode, MOSFET Parallelism, Synchronous Rectifier Buck Converter**

I. Introduction

Fundamentally, the body diode conduction losses, P_{BD} in the switch can be reduced by connecting several MOSFET in parallel. However, the level of reduction depends on the type and the number of switches used. Nevertheless, the analysis is yet to be comprehensive and has to be based on conduction modes. Therefore, this work is dedicated to investigate the potentials and disadvantages associated with multiple MOSFETs connected in parallel with respect to P_{BD}. Synchronous rectifier buck converter (SRBC) is applied as the test circuit where several different sets of parallel configurations of MOSFETs are used ranging from (S_1:1, S_2:1) to (S_1:4, S_2:4) for continuous conduction mode (CCM) operation. From the application of 1 MHz switching frequency, the outcomes of the study are explained in details.

A. MOSFETs Connected in Parallel

A number of MOSFET can be paralleled for the benefits of providing higher output current handling capability and hence the reduction in on-resistance of the rectifying path. Fig. 1 shows MOSFETs connected in parallel at S_1 and S_2.

The parallel connection of MOSFET allows for higher load current to be handled by sharing it between the individual switches. Because of MOSFET inhibiting a positive temperature coefficient, it can be paralleled without the need of source resistor. A single MOSFET can easily be heated up if it starts to draw slightly more current than the others. Therefore, its impedance will be increased which results in less current drawn. One way is to have paralleled MOSFETs to be mounted closer to each other so that the gate drive impedances are the same leading to the synchronized conduction [1-3].

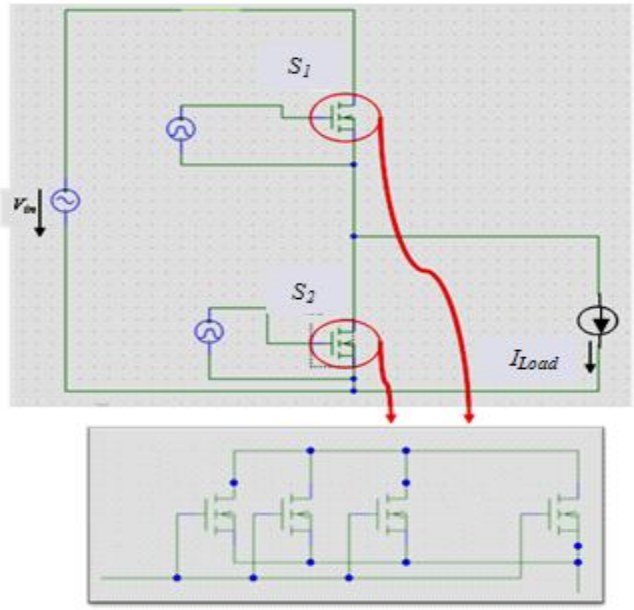

Fig. 1 MOSFETs Connected in Parallel

B. MOSFETs Connected in Series

MOSFET can also be connected in series to increase the voltage-handling capability. It is very crucial that the series-connected MOSFET are turned on and off simultaneously. Otherwise, the slowest device at turn-on and the fastest device at turn-off might be subjected to full drain-source voltage and that particular device will be destroyed due to excessive voltage [4-5]. The series connection of MOSFET is not preferred as it does not contribute to the increase of current at the load, unlike the parallel connection which is the interest in this work.

C. Body Diode Conduction Loss and Dead Time

When S_1 and S_2 are turned off, the parasitic body diode of S_2 is forward biased due to the continuity of I_L, and therefore an under-shoot of approximately - 700 mV is generated at node voltage, V_N [6] as shown in Fig. 2. This whole negative duration shows the duration of body diode conduction. S_2 can concurrently conduct with its body diode, creating stored charge that must be removed before it can support voltage. This eventually leads to high switching loss in S_1 and an increase in reverse recovery loss in S_2 body diode. Thus, S_2 is required to be turned off completely before S_1 starts to conduct during dead time, T_d, the duration when both S_1 and S_2 are not conducting. After T_d delay ends, S_2 will then start

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to conduct. As the forward voltage across S_2 is much lower than its body diode voltage drop, this will allow I_L to flow through it instead of S_1 [7]. Fig. 2 shows the body diode conduction interval measured at V_N.

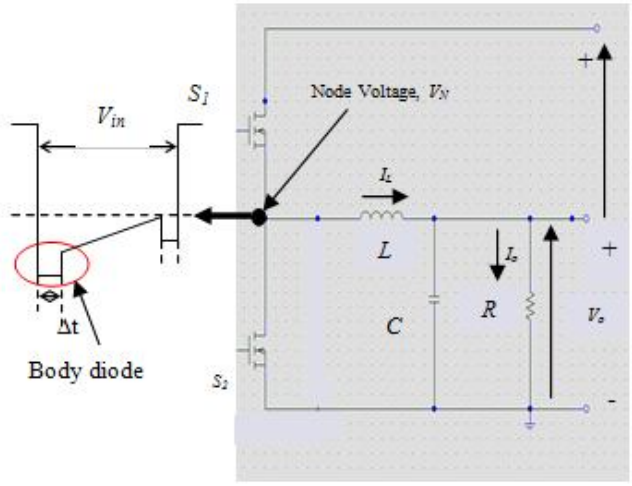

Fig. 2 Body Diode Conduction

The body diode conduction loss equation is represented by (1) where it is proportional to its conduction time. At smaller body diode conduction time, "t will have smaller body diode conduction losses. Therefore, in order to have a low P_{BD}, a shorter T_d is required [8].

$$P_{BD} = 2 \times V_F \times I_o \times f_s \times \Delta t \quad (1)$$

where V_F = body diode forward voltage drop, I_o = output current, f_s = switching frequency and
Δt = body diode conduction time.

D. Synchronous Rectifier Buck Converter

The S_2 switch of SRBC as shown in Fig. 3 is called synchronous rectifier since it only turns on after S_1 controlled switch is turned off. Once S_1 is turned back on, it then transfers the energy and charges the I_L to the load [9]. Incorrect synchronization of switches will increase P_{BD}.

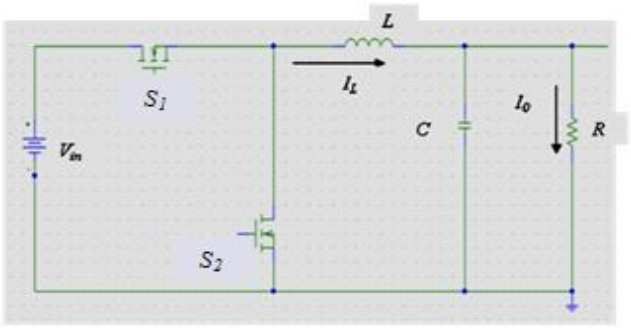

Fig. 3 Synchronous Rectifier Buck Converter

II. Methodology

A fixed pulse width modulation (PWM) signals are used in this work. The circuit configurations are constructed and simulated using PSpice software operating in 1 MHz switching frequency.

TABLE I
MOSFET PARALLELISM CONFIGURATION

S_1	S_2	S_1	S_2
1	1	3	1
1	2	3	2
1	3	3	3
1	4	3	4
2	1	4	1
2	2	4	2
2	3	4	3
2	4	4	4

Table I shows the configurations of MOSFETs connected in parallel as used in this work. There are 16 configurations to be studied. The configuration is indicated as (S_1:1, S_2:1) for example. That means, only one MOSFET at S_1 and S_2 respectively. If it is (S_1:3, S_2:4), there are three MOSFETs are paralleled at S_1 and four MOSFET at S_2 and so forth. The maximum is up to four for each S_1 and S_2.

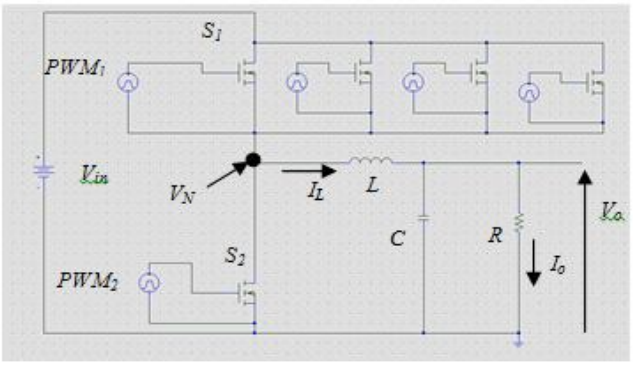

Fig. 4 Example of SRBC Circuit with MOSFET Parallelism for (S_1:4, S_2:1)

Fig. 4 shows four MOSFETs are paralleled at S_1 and a single MOSFET at S_2. First, the circuits are simulated. After that, to ensure that the settings of PWM_1 and PWM_2 are correct, voltage differential at both *PWMs* are measured. Then, V_N will be observed. At this point, V_N should be the same as input voltage, V_{in}. In addition, this point is also critical in observing the Δt.

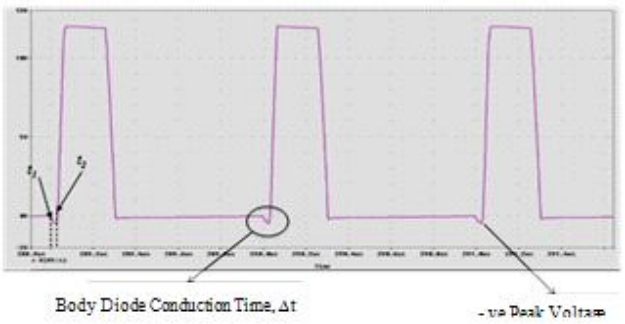

Fig. 5 Node Voltage, V_N in CCM for (S_1:4, S_2:1)

By putting voltage marker at V_N in the simulator, Δ t and negative peak are observed. The formula for calculating body

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diode conduction time is given in (2) which can be applied back to (1).

$$\Delta t = t_2 - t_1 \qquad (2)$$

III. Simulation Results & Discussions

Table II shows the summary of simulation results of SRBC circuit with paralleled MOSFET operating in CCM.

Table II. SRBC in CCM

Case (S_1:X, S_2:Y)	Node Voltage, V_N Δt (ns)	Negative Peak (mV)	Body diode Conduction Loss, P_{BD} (mW)
1, 1	53	-606.525	16.870
1, 2	54	-567.683	24.250
1, 3	55	-549.083	23.880
1, 4	55	-535.383	23.250
2, 1	49	-612.941	24.677
2, 2	50	-573.637	23.928
2, 3	49	-553.659	22.576
2, 4	60	-540.892	27.065
3, 2	30	-576.119	14.739
3, 3	30	-555.733	14.232
3, 4	50	-542.813	23.089
4, 1	20	-620.474	10.720
4, 2	49	-581.881	24.700
4, 3	48	-561.913	23.281
4, 4	30	-545.211	14.111

From Table II, the pattern of body diode conduction time can be observed. It can be noted that the body diode conduction time, "t is decreasing and fluctuating when the MOSFET parallelism technique is applied. Therefore, there are few configurations which have been determined to be the lowest range of P_{BD} as shown in Table III. The lowest P_{BD} range is found to be in (S_1:3, S_2:3), (S_1:4, S_2:1) and (S_1:4, S_2:4) combinations giving 14.232 mW, 10.720 mW and 14.111 mW respectively.

Table III
Configuration with Lowest P_{BD}

S_1	S_2
3	3
4	1
4	4

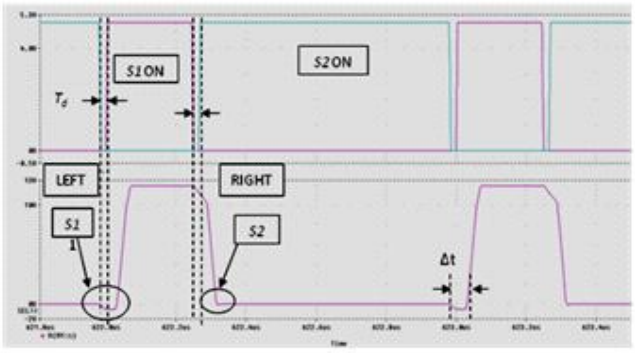

Fig. 6 Node Voltage, V_N in CCM for (S_1:4, S_2:1)

It is also determined that from Fig. 6, "t obtained from V_N comes from the switching of S_1 and S_2. On the left it shows the "t for S_1. This only occurs when S_1 is turned on. Whilst on the right is for S_2. Here, S_2 body diode is turned on with ZVS by circulating current that flows into L as soon as S_1 is turned off. For S_2, it is assumed that there is no P_{BD} when it conducts less than - 300 mV.

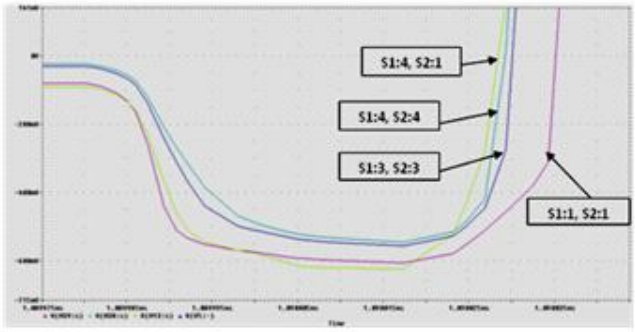

Fig. 7 Enlarged Body Diode Conduction Time in CCM for (S_1:4, S_2:1)

Fig. 7 shows the enlarged waveform of V_N of "t. There are three configurations which have the smallest "t such as 20 ns for configuration of (S_1:4, S_2:1), 30 ns for both configurations of (S_1:3×S_2:3) and (S_1:4×S_2:4). In Fig. 7, those three configurations are compared with the conventional configuration, (S_1:1×S_2:1). It is found that body diode conduction exists when the negative overshoot of node voltage has reached more than - 300 mV. Hence, it is an advantage to choose the negative peak voltage that is closest to this value. If the "t is smaller, it results in an increasing negative peak value. This can be seen in configuration of (S_1:4, S_2:1) having the negative peak of - 620.474 mV as referred to Table II.

On the other hand, the configuration of (S_1:4, S_2:1) has the shortest "t which is only 20 ns. More importantly, P_{BD} has been reduced by 36.45 % from 16.87 mW to 10.72 mW compared to (S_1:1, S_2:1).

Conclusion

This paper discusses on how much that MOSFET parallelism can affect the body diode conduction loss in SRBC circuit operating in CCM. It is found that the best configuration for CCM is when S_1 is paralleled with four MOSFETs and a single MOSFET at S_2. In this configuration, the body diode

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conduction loss has been eventually reduced by 36.45 % compared to conventional.

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